

**In the Claims:**

Please amend claims 2-4, 8, 9, 12-14, 16, 18-20, 24,25, 28-30 and 32. Please cancel claims 1, 5-7, 10-11, 15, 17, 21-23, 26, 27 and 31. Please add new claims 33-42.

The claims are as follows:

1. (Cancelled)

2. (Currently Amended) The integrated circuit device of claim [[1]] 33, further comprising a second circuit coupled to an output of said second latch and powered from said second rail.

3. (Currently Amended) The integrated circuit device of claim [[1]] 33, wherein said first clock phase signal is supplied from a first clock and said second clock phase signal is supplied from a second clock, said first and second clocks powered from a third power rail, said third power rail supplied from a third power supply.

4. (Currently Amended) The integrated circuit device of claim [[1]] 33, wherein:

    said first power rail is powered before said first clock phase signal goes high and is de-powered after said first clock phase signal goes low; and

    said second power rail is powered before said second clock phase signal goes high and is de-powered after second first clock phase signal goes low.

5-7 (Cancelled)

8. (Currently Amended) The integrated circuit device of claim [[6]] 34, wherein said first clock phase signal is supplied from a first clock and said second clock phase signal is supplied from a second clock, said first and second clocks powered from a third power rail, said third power rail supplied from a third power supply.

9. (Currently Amended) The integrated circuit device of claim [[6]] 34, wherein:

    said first power rail is powered before said first clock phase signal goes high and is de-powered after said first clock phase signal goes low; and

    said second power rail is powered before said second clock phase signal goes high and is de-powered after second first clock phase signal goes low.

10-11 (Cancelled)

12. (Currently Amended) The integrated circuit device of claim [[11]] 35, further comprising a fifth latch powered from said first power rail, said fourth circuit coupled to an input of said fifth latch.

13. (Currently Amended) The integrated circuit device of claim [[11]] 35, wherein said first clock phase signal is supplied from a first clock, said second clock phase signal is supplied from a second clock, said third clock phase signal is supplied from a third clock and said fourth clock phase signal is supplied from a fourth clock, said first, second, third and fourth clocks powered from a fifth power rail, said fifth power rail supplied from a fifth power supply.

14. (Currently Amended) The integrated circuit device of claim [[11]] 35, wherein:

    said first power rail is powered before said first clock phase signal goes high and is de-powered after said first clock phase signal goes low;

    said second power rail is powered before said second clock phase signal goes high and is de-powered after second first clock phase signal goes low;

    said third power rail is powered before said third clock phase signal goes high and is de-powered after said third clock phase signal goes low; and

    said fourth power rail is powered before said fourth clock phase signal goes high and is de-powered after second first clock phase signal goes low.

15. (Cancelled)

16. (Currently Amended) The integrated circuit of claim [[15]] 35, wherein said second clock phase goes high when said first clock phase goes low, said third clock phase goes high when said second clock phase goes low, said fourth clock phase goes high when said third clock phase goes low and said first clock phase goes high when said fourth clock phase goes low.

17. (Cancelled)

18. (Currently Amended) The method of claim [[17]] 36, further comprising a second circuit coupled to an output of said second latch and powered from said second rail.

19. (Currently Amended) The method of claim [[17]] 36, wherein:

said first clock phase signal is supplied from a first clock and said second clock phase signal is supplied from a second clock; and

powering said first and second clocks from a third power rail, said third power rail supplied from a third power supply.

20. (Currently Amended) The method of claim [[17]] 36, further including:

powering said first power rail before said first clock phase signal goes high and de-powering said first power rail after said first clock phase signal goes low; and

powering said second power rail before said second clock phase signal goes high and de-powering said second power rail after second clock phase signal goes low.

21-23. (Canceled)

25. (Currently Amended 1) The method of claim [[22]] 37, further including:

powering said first power rail before said first clock phase signal goes high and de-powering said first power rail after said first clock phase signal goes low; and

powering said second power rail before said second clock phase signal goes high and de-powering said second power rail after second clock phase signal goes low.

26-27 (Canceled)

28. (Currently Amended) The method of claim [[27]] 38, said integrated circuit further comprising a fifth latch powered from said first power rail, said fourth circuit coupled to an input of said fifth latch.

29. (Currently Amended) The method of claim [[27]] 38, wherein:

    said first clock phase signal is supplied from a first clock, said second clock phase signal is supplied from a second clock, said third clock phase signal is supplied from a third clock and said fourth clock phase signal is supplied from a fourth clock; and  
    powering said first, second, third and fourth clocks from a fifth power rail, said fifth power rail supplied from a fifth power supply.

30. (Currently Amended) The method of claim [[27]] 38, further including:

    powering said first power rail before said first clock phase signal goes high and de-powering said first power rail after said first clock phase signal goes low;  
    powering said second power rail before said first clock phase signal goes high and de-powering said second power rail after said first clock phase signal goes low;  
    powering said third power rail before said first clock phase signal goes high and de-powering said third power rail after said first clock phase signal goes low; and  
    powering said fourth power rail before said first clock phase signal goes high and de-powering said fourth power rail after said first clock phase signal goes low.

31 (Canceled)

32. (Currently Amended) The method of claim [[27]] 38, wherein said second clock phase signal goes high when said first clock phase signal goes low, said third clock phase signal goes high when said second clock phase signal goes low, said fourth clock phase signal goes high when said third clock phase signal goes low and said first clock phase signal goes high when said fourth clock phase signal goes low.

33. (New) An integrated circuit, comprising:

a first power rail connected to a first latch and a first circuit, said first power rail powered when a first clock signal is in an (A) state where A is equal to 0 or 1 and de-powered when said first clock signal is in a (1-A) state, said first power rail supplied from a first power supply;

a second power rail connected to a second latch, said second power rail powered when a second clock signal is in a (B) state where B is equal to 0 or 1 and de-powered when said second clock signal is in a (1-B) state, said second power rail supplied from a second power supply;

said circuit coupled between an output of said first latch and an input of said second latch; and

said first clock signal high whenever said second clock signal is low, said first clock signal low whenever said second clock signal is high.

34. (New) An integrated circuit, comprising:

a first power rail connected to an L1 latch of a first L1/L2 latch, to a first circuit and to an L1 latch of a second L1/L2 latch, said first power rail powered when a first clock signal is in an (A) state where A is equal to 0 or 1 and de-powered when said first clock signal is in a (1-A) state, said first power rail supplied from a first power supply;

a second power rail connected to an L2 latch of said first L1/L2 latch and to an L2 latch of said second L1/L2 latch, said second power rail powered when a second clock signal is in a (B) state where B is equal to 0 or 1 and de-powered when said second clock signal is in a (1-B) state, said second power rail supplied from a second power supply; and  
said first clock signal high whenever said second clock signal is low, said first clock signal low whenever said second clock signal is high.

35. (New) An integrated circuit, comprising:

a first power rail connected to a first latch and a first circuit, said first power rail powered when a first clock signal is in an (A) state where A is equal to 0 or 1 and de-powered when said first clock signal is in a (1-A) state, said first power rail supplied from a first power supply;

a second power rail connected to a second latch and a second circuit, said power rail powered when a second clock signal is in a (B) state where B is equal to 0 or 1 and de-powered when said second clock signal is in a (1-B) state, said second power rail supplied from a second power supply;

a third power rail connected to a third latch and a third circuit, said third power rail powered when a third clock signal is in a (C) state where C is equal to 0 or 1 and de-powered when said third clock signal is in a (1-C) state, said third power rail supplied from a third power supply;

a fourth power rail connected to a fourth latch and a fourth circuit, said fourth power rail powered when a fourth clock signal is in a (D) state where D is equal to 0 or 1 and de-powered when said fourth clock signal is in a (1-D) state, said fourth power rail supplied from a fourth power supply;

said first circuit coupled between an output of said first latch and an input of said second latch, said second circuit coupled between an output of said second latch and an input of said third latch, said third circuit coupled between an output of said third latch and an input of said fourth latch and said fourth circuit coupled to an output of said fourth latch; and

    either said first clock signal high whenever said second, third and fourth clocks are all low, said second clock signal high whenever said first, third and fourth clocks are all low, said third clock signal high whenever said first, second and fourth clocks are all low and said fourth clock signal high whenever said first, second and third clocks are all low or said first clock signal low whenever said second, third and fourth clocks are all high, said second clock signal low whenever said first, third and fourth clocks are all high, said third clock signal low whenever said first, second and fourth clocks are all high and said fourth clock signal low whenever said first, second and third clocks are all high.

36. (New) A method, comprising:

    providing said integrated circuit, said integrated circuit including:

        a first power rail connected to a first latch and a circuit, said first power rail supplied from a first power supply; and

        a second power rail connected to a second latch, said second power rail supplied from a second power supply, said circuit coupled between an output of said first latch and an input of said second latch;

    powering said first power rail when a first clock signal is in an (A) state where A is equal to 0 or 1 and de-powering said first power rail when said first clock signal is in a (1-A) state; and

powering said second power rail when a second clock signal is in a (B) state where B is equal to 0 or 1 and de-powering said second power rail when said second clock signal is in a (1-B) state, said first clock signal high whenever said second clock signal is low, said first clock signal low whenever said second clock signal is high.

37. (New) A method, comprising:

providing said integrated circuit, said integrated circuit including:

a first power rail connected to an L1 latch of a first L1/L2 latch, to a first circuit and to an L1 latch of a second L1/L2 latch, said first power rail supplied from a first power supply; and

a second power rail connected to an L2 latch of said first L1/L2 latch and to an L2 latch of said second L1/L2 latch, , said second power rail supplied from a second power supply;

powering said first power rail when a first clock signal is in an (A) state where A is equal to 0 or 1 and de-powering said first power rail when said first clock signal is in a (1-A) state; and

powering said second power rail when a second clock signal is in a (B) state where B is equal to 0 or 1 and de-powering said second power rail when said second clock signal is in a (1-B) state, said first clock signal high whenever said second clock signal is low, said first clock signal low whenever said second clock signal is high.

38. (New) A method, comprising:

providing said integrated circuit, said integrated circuit comprising:

a first power rail connected to a first latch and a first circuit, , said first power rail supplied from a first power supply;

a second power rail connected to a second latch and a second circuit, said second power rail supplied from a second power supply;

a third power rail connected to a third latch and a third circuit, said third power rail supplied from a third power supply;

a fourth power rail connected to a fourth latch and a fourth circuit, said fourth power rail supplied from a fourth power supply; and

said first circuit coupled between an output of said first latch and an input of said second latch, said second circuit coupled between an output of said second latch and an input of said third latch, said third circuit coupled between an output of said third latch and an input of said fourth latch and said fourth circuit coupled to an output of said fourth latch; and

powering said first power rail when a first clock signal is in an (A) state where A is equal to 0 or 1 and de-powering said first power rail when said first clock signal is in a (1-A) state;

powering said power rail powered when a second clock signal is in a (B) state where B is equal to 0 or 1 and de-powering said second power rail when said second clock signal is in a (1-B) state;

powering said third power rail powered when a third clock signal is in a (C) state where C is equal to 0 or 1 and de-powering said third power rail when said third clock signal is in a (1-C) state;

powering said fourth power rail powered when a fourth clock signal is in a (D) state where D is equal to 0 or 1 and de-powering said fourth power rail when said fourth clock signal is in a (1-D) state; and

either said first clock signal high whenever said second, third and fourth clocks are all low, said second clock signal high whenever said first, third and fourth clocks are all low, said third clock signal high whenever said first, second and fourth clocks are all low and said fourth clock signal high whenever said first, second and third clocks are all low or said first clock signal low whenever said second, third and fourth clocks are all high, said second clock signal low whenever said first, third and fourth clocks are all high, said third clock signal low whenever said first, second and fourth clocks are all high and said fourth clock signal low whenever said first, second and third clocks are all high.

39. (New) The integrated circuit of claim 33, wherin:

said first power rail is powered when said first clock is high and de-powered when said first clock signal is low and said second power rail is powered when said second clock is high and de-powered when said second clock signal is low; or

said first power rail is powered when said first clock is low and de-powered when said first clock signal is high and said second power rail is powered when said second clock is low and de-powered when said second clock signal is high.

40. (New) The method of claim 36, wherin said first power rail is powered when said first clock is high and de-powered when said first clock signal is low and said second power rail is powered when said second clock is high and de-powered when said second clock signal is low; or

said first power rail is powered when said first clock is low and de-powered when said first clock signal is high and said second power rail is powered when said second clock is low and de-powered when said second clock signal is high.

41. (New) The integrated circuit of claim 34, wherein:

    said first power rail is powered when said first clock is high and de-powered when said first clock signal is low and said second power rail is powered when said second clock is high and de-powered when said second clock signal is low; or

    said first power rail is powered when said first clock is low and de-powered when said first clock signal is high and said second power rail is powered when said second clock is low and de-powered when said second clock signal is high.

42. (New) The method of claim 37, wherein said first power rail is powered when said first clock is high and de-powered when said first clock signal is low and said second power rail is powered when said second clock is high and de-powered when said second clock signal is low; or

    said first power rail is powered when said first clock is low and de-powered when said first clock signal is high and said second power rail is powered when said second clock is low and de-powered when said second clock signal is high.